

Boundary-Scan and In-Circuit Test Combined: Strategy and Benefits

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Introduction

In-Circuit testing has long been the preferred testing method for most high volume manufacturers. In-Circuit testers are popular because they offer simple test generation, good fault coverage, fast test throughput, and diagnosis to the component pin level.

To achieve these benefits, In-Circuit testers have relied on bed-of-nails type fixtures that give the tester access to every component pin on the UUT. However, it is becoming increasingly difficult and expensive to design In-Circuit fixtures to access component pins on shrinking board designs.

Boundary scan components have testability logic built-in which can be used to test for PCB process faults as well as component functionality; therefore, many manufacturers have turned to a boundary scan test strategy to help them solve problem caused by loss of test access. Some have turned to boundary scan only test solutions, but these solutions are limited by the configuration of the boundary scan components on the UUT and do not provide the same level of fault coverage, throughput, and diagnostic accuracy as traditional In-Circuit tests.

An ideal solution is to combine the benefits of boundary scan test techniques with the benefits of traditional In-Circuit test techniques. Such a solution would continue to provide good fault coverage and diagnostics, but would require simpler and less expensive fixtures.

The following topics describe the benefits and issues of using a combined In-Circuit/Boundary Scan test strategy. They also describe board testability issues that should be considered to obtain maximum test fault coverage and diagnostic accuracy.

Fault Coverage Benefits

Testers that can only perform boundary scan tests, connecting to the UUT from an on-board connector, can miss a significant percentage of the manufacturing defects that may occur on a board. In-circuit testers are adept at detecting the following faults that can be missed by boundary scan only testers.

Shorted Nets

Boundary scan only testers can reliably detect shorts on pure boundary scan nets only. Shorts between boundary scan and non-boundary scan nets will only be detected when the non-boundary scan net is not in a high impedance state. Even if the short is detected, boundary scan only testers can not provide accurate diagnostic information that will aid the technician in the repair of the fault. By nailing conventional component pins, and using traditional In-Circuit shorts test techniques, these faults can be easily detected and diagnosed on both boundary scan and non boundary scan nodes.

Detecting all possible UUT shorts is an important benefit of the combined In-Circuit / boundary scan test strategy because:

- A significant number of possible shorts defects can escape if the test equipment can not detect shorts on non-boundary scan nodes.
- In-Circuit testing uses an un-powered test technique to detect shorts on nailed nodes; which prevents damage that could occur to a UUT when it is powered up with shorted nets.
- Undetected short faults between non-boundary and boundary scan nets can cause false failures of the boundary scan tests and inaccurate test diagnostics on boundary scan only testers (especially if the short involves a TAP net). These undetected faults can make it impossible to diagnose and repair the UUT

Mixed Component Nets

Boundary scan only testers can not detect faults on boundary scan nets that also have a connection to conventional digital tristate or bidirectional pin(s). This is because the boundary scan only tester has no way to control the conventional digital pin(s) and make sure that they do not interfere with the boundary scan interconnect tests. As a result, these mixed component nets must be removed from the boundary scan tests resulting in reduced fault coverage.

A combined In-Circuit / boundary scan test technique allows mixed nets to be tested because the conventional digital tristate and bidirectional pins can be preconditioned by driving control pins on the conventional devices, prior to the Interconnect test, using the tester Driver/Sensor technology.

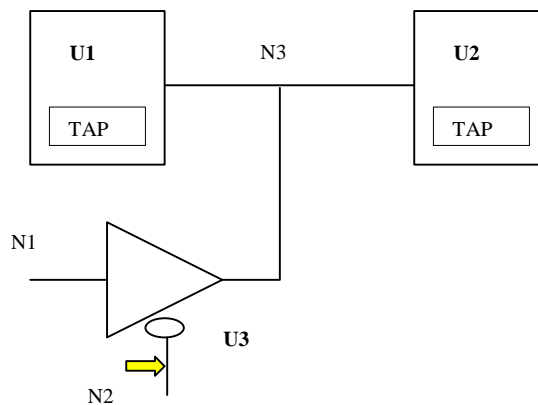


Figure 1

In Figure 1, node N3 cannot be tested during the boundary scan Interconnect tests unless the output from conventional component U3 can be shut off. With a combined In-Circuit/Boundary Scan tester, the U3 output is disabled by driving node N2 high with a tester Driver/Sensor nail.

Missing or Faulty Parts

Boundary scan only testers can not detect missing analog parts or conventional digital parts that do not have access to virtual boundary scan drivers and sensors. With most board designs, this will result in a significant loss of test fault coverage.

By providing 'bed-of-nail' access to the nets that contain these parts, and using standard In-Circuit test techniques, missing or faulty non-boundary scan parts can be detected, test fault coverage improved, and diagnostic accuracy enhanced.

In-Circuit Hardware Benefits

In-Circuit testers come with a number of standard hardware features that are not available in simple boundary-scan only testers. These hardware features can be used to simplify development and improve the fault coverage of boundary scan tests.

Driver/Sensor Technology

In-Circuit testers come equipped with sophisticated Driver/Sensor technology. The powerful Driver/Sensors can be used in the following ways during boundary scan testing.

- In-Circuit Drivers are capable of supplying very high drive currents, usually greater than 500mA. This capability can be used to backdrive, or force, device nodes to the voltage required by the boundary scan tests. This capability is fundamental to boundary scan interaction tests, which are used to detect shorts between nailed conventional nets and un-nailed boundary scan nets. The high current capability of the In-Circuit Drivers can also be used to avoid programming scan path selector and bridge devices, because the Drivers can directly backdrive the outputs of these devices. Finally, In-Circuit Drivers can be used to drive multiple UUT scan paths simultaneously. This comes in handy when the board was designed with multiple scan paths or when boundary scan chains must be divided because one or more boundary scan parts does not comply with the IEEE 1149.1 standard.

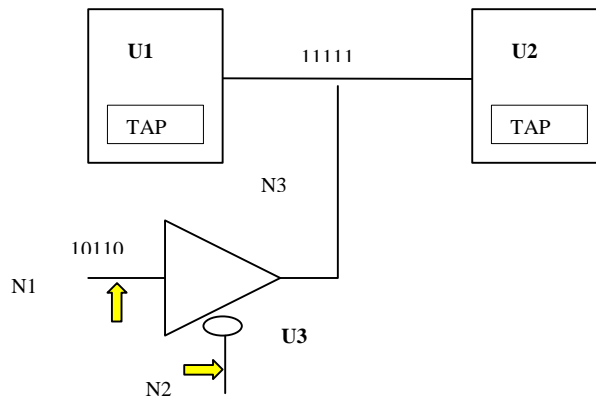


Figure 2

In Figure 2, a short between nailed conventional node N1 and un-nailed boundary scan node N3 can be detected by programming the U1 boundary scan output to drive all ones, and by driving a node identifier on N1 using the tester Driver/Sensor nail. If the U2 boundary scan input captures the N1 node identifier, instead of all ones, then a short exists between the two nodes. This test technique relies on the fact that the driver technology has enough current capability to backdrive the boundary scan outputs. During the test U3 is disabled by driving node N2 high with a tester Driver/Sensor nail.

- Most In-Circuit testers have hundreds, if not thousands, of Driver/Sensor pins. These drivers can be used to precondition critical UUT signals prior to the start of the boundary scan tests. For example, In-Circuit drivers can be used to ensure that all boundary scan compliance enable pins are driven to their enable values. The drivers can also be used to ensure that non-boundary scan components are shut off so that they do not interfere with the boundary scan tests. Special tooling boards must be designed on boundary scan only testers to accomplish the same objectives.
- Most In-Circuit Drivers have programmable voltage values. This capability is useful when the board is designed with technologies that require several different logic levels. Programmable drive levels also help when trying to debug electrical problems related to ground bounce or ringing TAP signals.

Automatic Isolation

Most In-Circuit testers have Automatic Test Generation (ATG) software that is used to generate tests for components on the board. The ATG software relies on device libraries that describe how to test and isolate individual components.

Combined In-Circuit / boundary scan testers can take advantage of the built-in ATG software to isolate all conventional UUT components during the boundary scan tests. This minimizes the chances of false failures during the boundary scan tests due to non-boundary scan device interference.

The best In-Circuit/boundary scan test solutions will also utilize boundary scan commands to shut off all boundary scan devices at the beginning of powered-up conventional device tests. This reduces the chances for false failures and intermittent test results due to on-board signal activity.

Analog Stimulus and Measurement Instruments

In-Circuit testers come equipped with analog stimulus and measurement instruments that are not available on boundary scan only testers. These instruments can be scanned to any D/S resource in the tester so that instrument connections do not have to be hardwired in the test fixture.

Combined In-Circuit/boundary scan testers can make use of these instruments to improve fault coverage and diagnostics of the test program. For example, the analog instrumentation can be used to verify that the UUT power supply voltages are correct, that critical analog components are installed, and that the board is running at the designed frequency.

Programmable UUT Power Supplies

In-Circuit testers come equipped with power supplies that can program voltage and current parameters for the board under test. This capability allows automatic generation of safe UUT power-up, power-down, and discharge routines. Most boundary scan only testers do not provide programmable power supplies, and the UUT must be powered up using separate, stand-alone power supplies.

Automation Ready

In-Circuit test systems are designed to integrate into high volume automated manufacturing lines. Features of the tester, like vacuum or compression actuated fixtures, paperless repair software, data logging software, panel test software, and compliance to SMEMA specifications enable In-Circuit testers to adapt to the highest throughput automated manufacturing facilities.

Debug Issues

One of the major advantages of boundary scan over traditional in-circuit vector testing is that, provided the information about the testability circuitry is correct (BSDL), and the boundary scan components comply with the IEEE 1149.1 standard, then the program developed will work without debug. This is due to the fact that the boundary scan test software knows how all boundary scan components will behave when they are in test mode.

Boundary scan tests rely on ALL devices in the chain being compliant and described correctly. A single non-compliant device or inaccurate BSDL description can cause all boundary scan tests to fail. To complicate debug further, the test engineer may only have prototype boards that will often contain undiagnosed design and manufacturing defects.

There is an added practical complication: Boundary scan tests are used because there is incomplete physical access to the board, and so the only visibility to what is happening may be through the test logic in the boundary-scan devices or with an oscilloscope triggered from the tester.

The boundary scan debug process is much different than traditional in-circuit debug. Having test point access to all nets, as in in-circuit test, makes debug a simpler process than when only partial net access is available. The person doing boundary scan debug must not only have a good understanding of in-circuit debug techniques but also a knowledge of the boundary scan IEEE 1149.1 specification and of the hierarchy of boundary scan tests generated by the boundary scan software. The person assigned to debug the boundary scan/in-circuit test must use a block diagram approach to 'bringing up' the board. They must rely on test sequence knowledge to logically determine possible causes of the boundary scan test failures.

The most common reasons for boundary scan test failures are listed below, along with debug actions that can be used on a combined In-Circuit / boundary scan tester to resolve them.

BSDL Inaccuracies

A BSDL model contains many facts about what the test circuitry in the boundary scan part does. A typical 250-pin boundary-scan part will have about 400 facts in the BSDL model. Any fact being wrong can cause one test (or many tests) to fail.

Finding mistakes in BSDL models with loaded board tests is extremely difficult, particularly if the board has many boundary scan devices. Each test brings together data from all of the BSDL models for the board, plus netlist and fixture information. Data in each of the BSDL models can be used dozens of times, in dozens of tests. If any data fact is wrong, many tests can fail in complex ways.

Unless there is very good reason to be certain that the BSDL is correct (e.g. it has been produced automatically by a synthesis tool and never altered, or it has been used with success on other boundary scan tests) it should be regarded as untrustworthy.

To avoid complex debug activities caused by inaccurate BSDL models, each BSDL model should be verified by generating boundary scan tests to test a single device. In-Circuit testers usually offer BSDL verification software that can verify the accuracy of the BSDL model by using a device modeling fixture and the built-in tester D/S resources. The BSDL verification software is capable of detecting a mismatch between device behavior and data facts in the BSDL model.

Failure to adequately check out BSDL models prior to generation of the boundary scan tests can cause much wasted time.

Isolating Conventional Components

Boundary scan nets that are connected to conventional digital output or bidirectional pins can fail boundary scan Interconnect tests. This can occur when the conventional digital output driver is not shut off and conflicts with the value that the boundary scan output is attempting to drive the net.

In order to reliably test these nets, the conventional digital output or bidirectional pins must be effectively disabled by placing them in the high impedance state. This can be effectively accomplished on in-circuit testers by driving control pins of the conventional device to values that will disable these pins.

As previously mentioned, In-Circuit testers also have software libraries for common commercial components that describe how to isolate or disable device pins. So, if the tester has access to the control pins of the conventional component, and a model for the component is present in the device libraries, then the automatic test generation software will automatically include the appropriate isolation sections.

When the tester does not have access to the control pins of the conventional component, then these nets can not be reliably tested and the test programmer should remove them from the boundary scan tests and suffer the resulting drop in test fault coverage.

If the tester has access to the control pins, but is missing isolation sections because there is no device model for the conventional component, then the boundary scan test is likely to fail or be intermittent. In this case, the test programmer should create a device model for the conventional component that includes isolation information, or add the isolation code directly to the test program during debug to resolve the problem.

Electrical Problems

The TCK signal(s) for Boundary Scan parts is the most important signal. It is an essential part of the test equipment that is testing the board. If it is noisy, ringing or otherwise unreliable, many tests will fail badly. Noise on the TCK signal will cause the boundary scan test hardware to lose synchronization with the test hardware (the boundary scan TAP controllers will be in a different state than the tester expects or will capture or drive incorrect data).

If the test programmer is fortunate, problems with the TCK signal(s) will be detected during the boundary scan hardware integrity tests, where they will be easy to detect. More than likely, however, problems with TCK signal(s) will cause boundary scan tests to

fail in unreliable ways. Electrical problems that affect boundary scan tests usually fall into one of these categories:

- **Ground Bounce** - Ground bounce is one of the nastiest problems that can occur on a board. It is caused by bad component design, or by a poor power and ground distribution in the board or fixture.

Boundary scan tests are the ones most likely to bring ground bounce susceptibility into the open, because boundary scan tests, by their very nature, will change many device outputs at the same time. In addition shorts to un-nailed nets may be discovered when changing device outputs, which can cause large current changes that were not anticipated by the designer.

Some chip designers claim that boundary scan tests should not change too many outputs in a device at the same time. This claim violates the 1149.1 standard that states that devices must be able to handle any set of requested output changes.

There is in fact no way for any test generator to avoid unlimited numbers of simultaneous changes because the change into EXTEST operation is a change from normal operation (when the boundary scan hardware is transparent) to EXTEST (where the device outputs are controlled by the boundary scan hardware).

Some boundary scan test solutions precondition the TMS signal prior to the transition into the Update-IR or Update-DR TAP state so that extra transitions of the TCK pin caused by ground bounce will cause the boundary scan state machine to stay in Run-Test/Idle state. By using Run-Test/Idle as the start and stop state, synchronization problems related to ground bounce are minimized.

- **Signal Reflections** – Digital transmission line theory teaches that as the frequency and slew rate of a digital signal increases, the more likely it is for ringing to occur, and the more important it is to have a matched network impedances to prevent signal reflection.

If the TCK signal is being driven by the output of an on-board device, then it may have a very fast slew rate that can cause ringing. If the TCK net is also attached to a tester D/S resource, then the ringing effect will be magnified by the effects of a the fixture wire attached to the net.

This problem can be resolved in several ways on combined In-Circuit / boundary scan testers. If you have access to the TCK signal(s), you can disable the output pin that is driving the TCK signal and drive the TCK nets directly with the tester D/S resources. This approach allows the test programmer to control the slew rate, voltage, and frequency of the TCK signal(s) for best results.

If the above approach can not be used, then the test programmer can remove the fixture wire(s) attached to the TCK signal(s) to reduce signal reflections caused by the wires that are attached to the net.

Non-Compliance

Boundary scan tests, and the methods for using boundary scan, are based on an important assumption: there is correctly functioning boundary-scan circuitry in the

components. The general meaning of **correctly functioning** is that the devices obey the IEEE 1149.1 Standard. Unfortunately there are a significant number of devices that fail to adhere to the Standard, and often the problems this causes are regarded as problems with the test tools, rather than the components.

Non-Compliant parts can easily mean that there is no chance of using a boundary-scan based test strategy, or that excessive work will be needed to implement such a strategy. It is often hard to discover non-compliance from documentation, non-compliance will be mentioned in small footnotes or not at all. It is worth noting that BSDL cannot describe non-compliant behavior. The reason is simple: permitting the description of such behavior would imply that it is actually acceptable and make it impossible for test vendors to supply general purpose boundary scan test generation software.

One place that non-compliance is sometimes documented is in comments in BSDL descriptions. When someone is writing BSDL and finds some things that they cannot describe they will add comments describing the device behavior that cannot be described.

There are three general strategies for handling non-compliance: modifying the BSDL file to describe a compliant subset of device behavior, altering the tests that are produced by the test generators, or modifying the board circuit description.

- **Modifying the BSDL** – Changing the BSDL file to describe a compliant subset of device behavior is the simplest method of dealing with non-compliant device behavior, but it does require understanding of the BSDL language and what the 1149.1 Standard permits.

As an example, a non-compliant boundary scan device may not support the mandatory SAMPLE/PRELOAD instruction. A knowledgeable test programmer could choose to edit the BSDL model and specify the EXTEST instruction as a suitable replacement for the SAMPLE/PRELOAD instruction.

- **Altering the Boundary Scan Tests** – If the test programmer can determine in what ways a device is non-compliant, and a method of working around the non-compliance, then they can edit the tests that are generated by the boundary scan test generators to work around the non-compliant behavior.

For example, if a boundary scan device needs an additional clock in addition to the TCK clock, for the boundary-scan circuitry to work; then the test programmer could edit the generated boundary scan tests to make sure the board or the tester generates the extra clock.

This approach can become tedious because the editing changes must be made to each boundary scan test and have to be repeated each time the test programmer re-generates the boundary scan tests. Also, this approach can only be used when the test solution supports a general-purpose programmable test language.

- **Modifying the Circuit Description** – If a device consistently misbehaves during boundary scan tests and the test programmer cannot determine the cause of the non-compliance, then they could choose to ignore the device altogether by telling the software that the part is not really part of the boundary scan chain.

Doing this effectively changes the boundary scan chain description and forces the test generator to test the board using multiple scan paths. This approach only works if you are using a combined In-Circuit / boundary scan test strategy and the tester has access to the internal TDI/TDO nets on the board.

Removing boundary scan devices from the scan path description should only be pursued after the others have failed because it results in reduced test fault coverage.

Access Decisions

To obtain the benefits of a combined boundary scan / In-Circuit test strategy, you must determine where access is critical and build a test fixture that provides access to critical component pins on the UUT. The amount of access required, and the complexity of the fixture will depend on the amount of pure boundary scan nets on the board and what your test strategy is for testing non-bscan components. In general, you should provide access to the following locations on the board.

Test Access Port Nets

At a minimum, tester access must be provided to drive the board TMS, TCK, TRST, and primary TDI/TDO signals. Without access to these Test Access Port nets, it is impossible to implement a boundary scan test strategy. These are the only signals that many boundary scan only testers are capable of driving.

Compliance Pins

Many boundary scan components have IEEE 1149.1 Compliance Enable pins. These Compliance Enable pins must be driven either high or low throughout the boundary scan tests or else the component will not comply with the 1149.1 standard.

Access to all Compliance Enable pins is imperative. Failure to drive or tie these pins to the required compliance enable state makes it impossible to use a boundary scan test strategy.

Non Boundary Scan Nets

Tester access should be provided to nets that can not be driven or sensed using boundary scan pins. Failure to provide tester access to these nets could limit test fault coverage dramatically because none of the components attached to the net could be tested.

Furthermore, when access is not provided on these nets, it is not possible to shut off conventional component output and bidirectional pins when executing the boundary scan tests, thus limiting test fault coverage further.

Critical UUT Control Signals

To improve test reliability and control, you should consider providing tester access to critical board control signals. Doing so will make it easy to quiet the board during debug and test without relying on possible faulty boundary scan components to provide the important signals.

Intermediate TDI/TDO Nets

Providing access to intermediate TDI/TDO signals is not required, but provides additional test benefits in three areas.

- **Better Diagnostic Accuracy** – Providing tester access to the internal TDI/TDO signals allows the standard In-Circuit shorts test to automatically detect any shorts between these TAP signals and other nailed nets on the board. Shorts associated with unnailed TAP signals are notoriously difficult to detect and diagnose and generally cause unreliable operation of the boundary scan tests.

When the tester has access to the internal TDI/TDO signals on a board then multiple faults can also be detected in the board scan path. For example, if there are multiple opens between internal TDI/TDO signals, then the tester would be able to report all opens in the scan path. Testers that only have access to the last TDO signal would only be able to report the location of the open in the scan path that was closest to the TDO signal.

- **Control of Scan Path Signals** – When the tester has access to all the board TAP signals, then the test programmer can directly control which board nets are used to drive the scan path TAP signals.

For example, the board may have a scan path selector or bridge chip that must be programmed to configure the scan path prior to executing any boundary scan tests. The complexity of the additional programming could be avoided by ignoring these devices and telling the tester to drive the TAP signals of the boundary scan devices directly.

- **Debug Flexibility** – When the tester has access to all board TAP signals, the test programmer can decide to break up the scan path to get around non-compliant boundary scan components.

For example, if the test programmer discovers a non-compliant boundary scan component, they can decide to remove it from the scan path and use multiple scan paths to test the board.

Summary

Manufacturing densely packed Printed Circuit Boards with boundary scan components allows test engineers to maintain high fault coverage with limited test access. However, test solutions that only employ boundary scan test techniques can cause many manufacturing defects to escape detection. Table 1 shows that a test approach that combines boundary scan test techniques with traditional In-Circuit test techniques provides the best test fault coverage and most accurate diagnostic information.

Defect	BSCAN Only	ICT Only	Combined BSCAN/ICT
Shorts between unnailed Pure Bscan Nodes	✓		✓
Shorts on unnailed mixed component nets			✓
Shorts between unnailed Bscan nets and nailed non-Bscan nets			✓
Shorts between nailed non-Bscan nets		✓	✓
Opens on unnailed Pure Bscan nets	✓		✓
Opens on nailed single pin Bscan nets		✓	✓
Missing or faulty non-Bscan parts	Only if non-bscan part can be tested using bscan pins as virtual drivers and sensors	✓	✓
Missing or faulty Bscan parts	✓	Only if bscan parts are nailed	✓
Fixture Cost / Diagnostic Accuracy			
Fixture Cost	Low	High	Medium
Diagnostic Accuracy	Poor. Cannot diagnose faults on non bscan nets	Excellent, but all nodes must be nailed	Good. Can diagnose faults on nailed and unnailed nodes

Table 1

Acknowledgements:

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