50621

The Buried Capacitance Design Guide

HADCO

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1.0 Introduction

SANMINA Corporation's Buried Capactance™ (BC) technology provides a cost effective approach for decoupling high performance printed circuit board components and reducing electro-magnetic interference (EMI). Utilizing this internal power/ground plane construction can eliminate the need for or enhance the performance of Integrated Circuit (IC) decoupling capacitors.

This Design Manual provides information for design engineers, EMI/EMC engineers and PCB fabricators to effectively utilize the BC technology.

The guide is divided into the following sections:

2.0 High Speed Decoupling Strategy

A discussion of high performance IC decoupling techniques.

3.0 EMI/EMC Control

A presentation of how BC can assist in reducing EMI emissions.

4.0 Distributed Capacitance Approach

A discussion of how to effectively utilize the Buried Capacitor technology.

5.0 Buried Capacitance Technical Specification

This contains the BC-2000™ material and fabricated board technical specifications.

6.0 Additional Buried Capacitance Benefits

Presentation of non-decoupling benefits that can be obtained with the use of BC technology.

A Appendices

Supporting information for the technical sections.

2.0 High Speed Decoupling Strategy

Providing power to high speed integrated circuits (IC's) requires a solid DC and AC power distribution network overlaid on each other. To properly design a highly efficient power distribution system each impedance component must be determined. Decoupling capacitance must be distributed near the required loads to provide high speed current that is not provided by the existing system.

2.1 Power Plane Impedance

The power plane distribution planes utilized in multilayer backplanes and daughterboards do not have zero impedance. It is a combination of DC resistance and AC impedance. The DC and AC elements reduce the voltage that is available for the components. This can be mathematically expressed as,

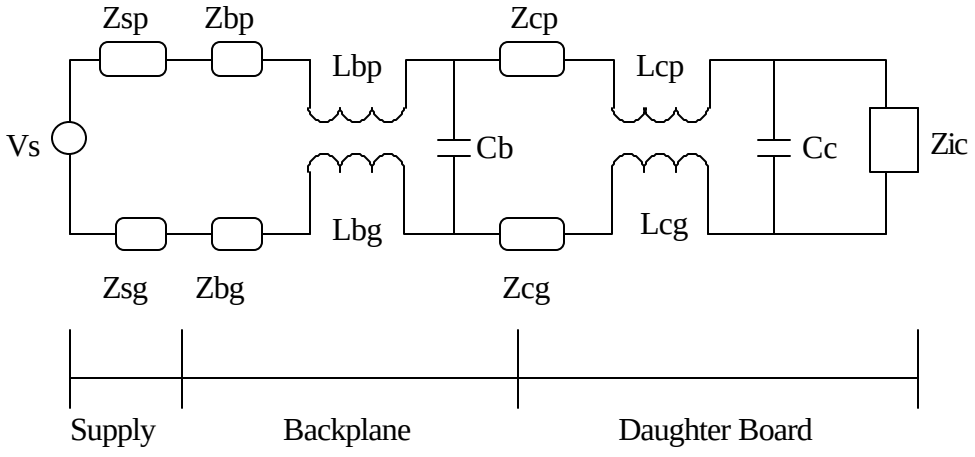
$$V(t)_{Load} = V_S - (V_{DC} + V_{AC}(t)) \quad 1)$$

Where, $V_{DC} = I_{DC}(R_{Supply} + R_{Backplane} + R_{PCB})$ 2)

$V_{AC}(t) = I_S(t)(Z_{Supply} + Z_{Backplane} + Z_{PCB})$ 3)

The time dependent voltage drops are determined by the amplitude, phase relationships and frequency components required by the IC's. $V_{AC}(t)$ is the result of the AC current requirements times the power distribution AC impedance. This will be discussed in more detail in this guide. The $V_{DC} + V_{AC}(t)$ term is defined as the noise margin. The component supplier should specify the net voltage that is required at the load. Typically, the AC noise component can be higher than the listed DC noise margin, but is not specified on the component data sheet.

A high level lumped element model of a multilayer distribution network is shown in Figure 1. The distribution impedance are sub-divided as power supply, backplane and daughterboard impedance which are each composed of inductance, resistance, and capacitance.



System Level Decoupling System Model
Figure 1

In larger systems power is provided by the DC power supply (V_s) to a backplane through cables and connectors. The cables have inherent impedance in both the power rail (Z_{sp}) and the ground rail (Z_{sg}).

The backplane is composed of many connectors with the DC power being distributed via internal planes. The power planes have distributed impedance on the voltage (Z_{bp}) and ground (Z_{bg}) rails and inherent and mutual inductance (L_{bp}, L_{bg}) properties which provide resistance to the current flow. They also have inherent lossy properties for current requirements at high frequencies.

The PCB, like the backplane has similar properties, in that the current is provided through lossy connectors (Z_{cp}, Z_{cg}), and power planes with distributed capacitance and inductance (L_{cp}, L_{cg}) on both the voltage and ground rails.

When the internal components within the packaged IC require current it must be provided through all of these components at the required time. Before determining how to negate these barriers a more detailed discussion on the DC and AC distribution networks will be presented.

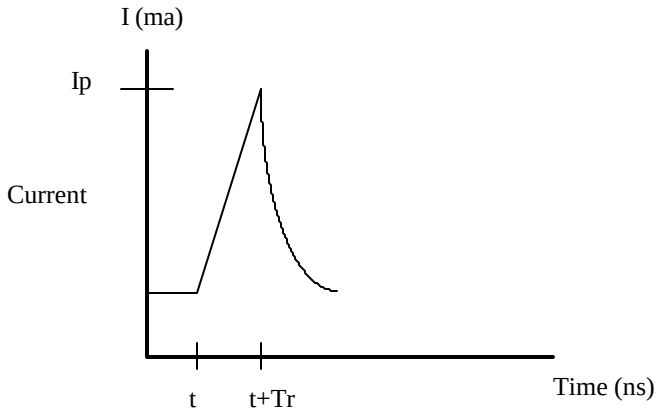
2.2 IC Switching Current Model

The current requirements for each component must be identified to properly assess the decoupling and power distribution requirements. In a generic sense, the current requirements can be classified into the following categories:

- Quiescent : Steady-state device current
- Output Capacitive Load : Capacitive load charging current
- Transmission Line Load : Transmission line load current
- Device Output charge : Device output state change switching current
- Cyclic Switching : IC decoupling capacitance recharge current

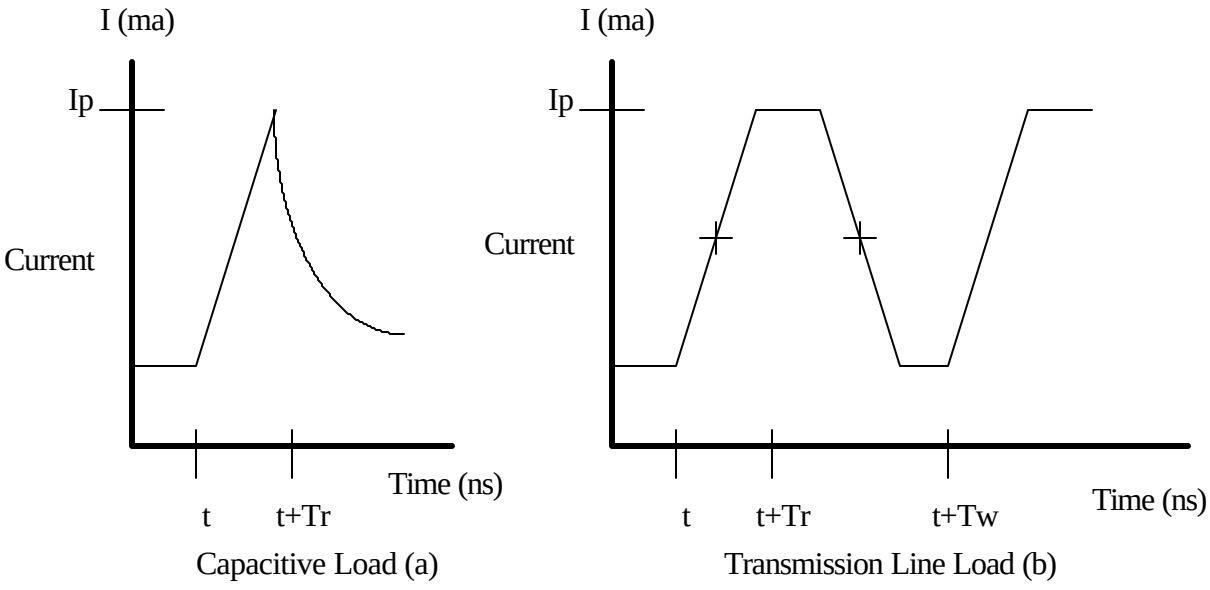
Decoupling capacitors have definitive response times and frequency responses. To effectively determine the power distribution characteristics, the output switching pulse, Figures 2 & 3, and the Fourier transform, Figure 4, can be utilized. The current waveform illustrated in Figure 2 presents the supply current required to power the internal IC circuitry and provide current to output switching stages. This does not take into account the output loads.

As will be presented later, the decoupling system components have specific current supply versus frequency response characteristics.



Typical Output Switching Current Waveform
Figure 2

The output current pulses will be modified by the time dependent current sourcing requirements of the loads. This current provides switching current to the signal line and connected loads. This current is provided until it reaches its quiescent state. If insufficient capacitance/current is provided, the edge transition time (T_r) will degrade.

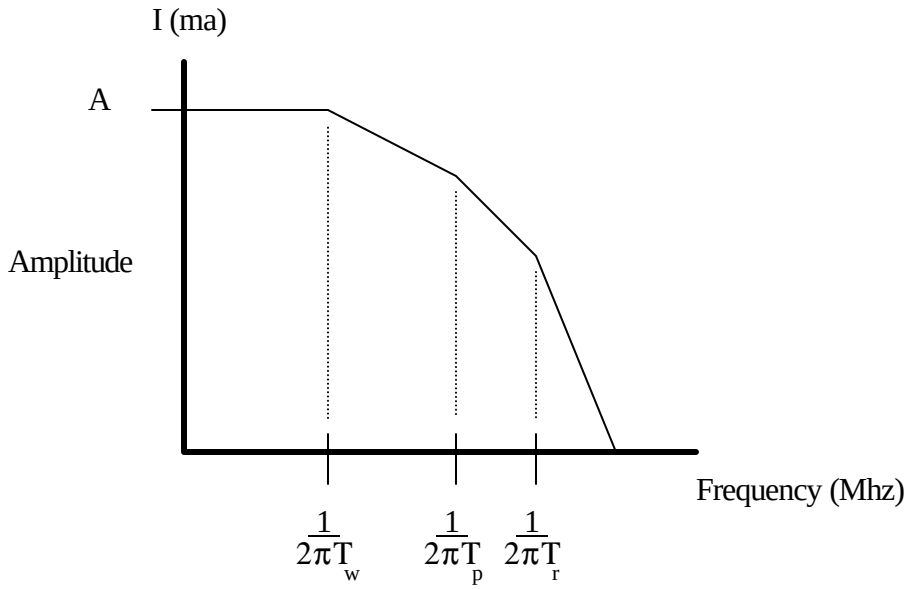


Typical Capacitive and Transmission Line Load Current Waveforms
Figure 3

Two types of line charging currents are required: **capacitive line** and **transmission line**.

Capacitive line charging requires a relatively slower charging rate than a transmission line, but must provide more current. It is characterized by a conventional RC time constant charge/decay model, Figure 3a.

A transmission line requires a slower, lower amplitude, but typically longer, current pulse to keep the line charged until all of the reflections are over. It is more characteristic of a network which has capacitance at both ends and a resistive central element, as presented in Figure 3b. T_r is the pulse risetime (10 - 90%). T_p is the transmission line current pulse required for a single down-and-back propagation time measured at the 50% point. T_w is the clock period and is also measured at the 50% point.

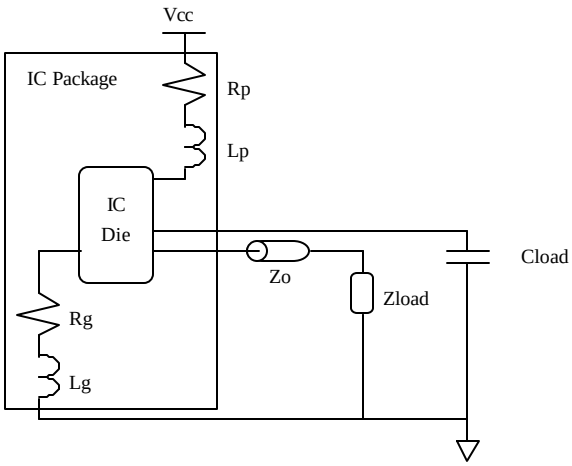


Typical Output Switching Current Fourier Transform
Figure 4

2.3 IC Package Impedance Model

IC's must be mounted and connected to the PCB. This is accomplished using many packaging techniques, e.g., TAB, COB, MCM, PLCC and SOIC. In each of these configurations there are physical connections which introduce resistance, inductance and capacitance into the power distribution path.

Also complicating this are the various types of load configurations which require switching and charge current to be provided through the ICs power leads. Figure 5 presents a high level device decoupling model. R_p and L_p represent the impedance components for the power lead(s) of the device package and bond wires. R_g and L_g represent the impedance components for the ground lead(s) of the device package and bond wires. C_{load} is the combined capacitance of the package lead, signal trace and the input load capacitance for the attached devices. For a transmission line load Zo represents the trace transmission line and Z_{load} represents the input impedance of the attached loads. The impedance model can be very complex, based on the actual topology of the network.



Integrated Circuit Package and Load Model
Figure 5

The component model for each of these elements is unique with respect to its physical implementation. Each of the loads, or current demands, may be synchronous or asynchronous. Thus, the high frequency current demands that the power grid must provide are very complex and must be analyzed starting at an architectural level then broken down to the finite device model. The time varying current demands in conjunction with the voltage drop budget must be overlaid onto the DC and AC power distribution characteristics to determine the optimum decoupling system design.

2.4 DC Resistance

The underlying component of the power distribution system is the DC distribution. By definition it is time invariant. When analyzing the AC power supply requirements for a component, the DC voltage drop, or budget, is only considered to determine the basis, at each component, for determining the voltage drop budget allowance for the AC component.

We will not analyze the DC resistance component, other than to point out where the most significant losses will usually occur.

- Cables - Cable volume resistivity
  - Connector inherent and contact resistance
- Backplane (B/P) - PCB-B/P contact pins and pin location relative to the load
  - Connector inherent and contact resistance
  - Power plane net sheet resistance (base copper area less
    - component clearance holes)
- PCB - Connector inherent and contact resistance
  - Power plane net sheet resistance (base copper area less
    - component clearance holes)

The static voltage drop between any two points on a copper plane is determined by multiplying the maximum load current by the plane sheet resistance, Rt.

$$R_t = 679/ T_p \quad \mu\Omega/\text{square}$$

where, T_p = thickness of plane (mils)

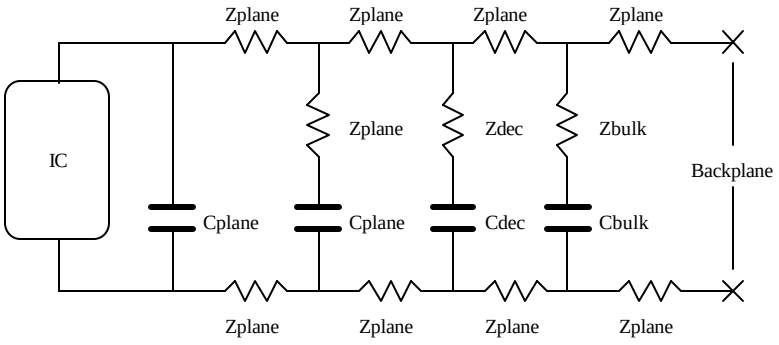
A model analysis is used to determine R_t between each integrated circuit location. A computer program, such as P-SPICE should be utilized to simplify the analysis. Each device is modeled as a point load and each connector pin is treated as a point source.

2.5 AC Impedance

More than the DC component, the AC impedance is very sensitive to the physical connectivity and physical shape/size of the power distribution system.

The power supply to PCB path is very complex. To simplify the discussion let's breakdown the PCB component into finer granularity. The PCB power distribution path starts at the edge of the connector interface. Power is distributed across the board in the power plane to the component and returns to the connector, typically on another plane. There are several capacitance elements distributed between these planes which provide high frequency current which can't be provided by the power supply due to the various AC impedance inherent to the distribution system.

The PCB power distribution AC impedance is subdivided into three components as shown in Figure 6. The highest frequency component is C_{plane}. This is the capacitance created by the power plane pairs. On a finite basis this plane is the area directly under the IC and the area halfway between it and adjacent ICs. Additional plane area is available when adjacent devices do not require current simultaneously. This will be discussed in more detail in Section 4. The planes distributed capacitance provides the highest frequency decoupling component. It's response time and losses are determined by the planes inductance, mutual inductance and DC resistance.



PCB Decoupling Model
Figure 6

The first decoupling component is the power plane capacitance, C_{plane}. This capacitance is formed by the adjacent Vcc and ground power planes. The dielectric is a resin, such as FR-4, with a glass reinforcement. The planes provide low

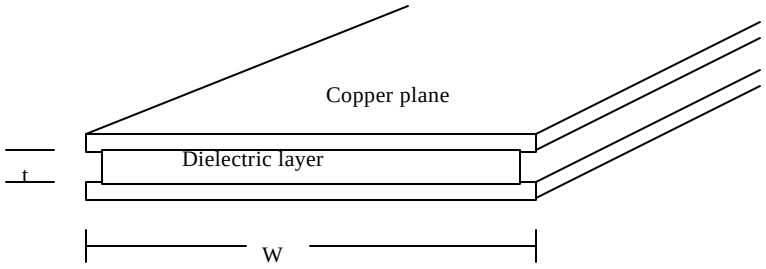
capacitance, on the order of 50 to 506 pf/in^2. Since the dielectric is polymeric its frequency response is very fast, thus allowing it to decouple very high frequency components. Typically it will provide current fast enough for the initial edge transition and the capacitive and transmission line loads. As the local plane capacitance is depleted then current is drawn from the plane further away from the device. This current will be partially negated by the planes inherent impedance.

The second decoupling component is the IC decoupling capacitor C_{dec}. These capacitors are generally located next to every, or every other, IC on the PCB. It is intended to provide the switching, and load charging current that is required from the IC. Its impedance is generally due to the internal plate and lead inductance and resistance. Lead inductance in lowered by the use of surface mount capacitors versus axial or radially leaded components.

The final decoupling component is the bulk capacitor, $C_{bulk,}$ which recharges the ICs decoupling capacitors and power plane. The current in this impedance is lower in frequency and higher in amplitude than the current in the first component. The voltage drop due to the lower impedance, because of the lower frequency involved, will be less than the above case.

2.5.1 Power Plane Capacitance Model

The power plane distribution is composed of two, or more, internal PCB planes, Figure 7. Each pair provides one power and one ground return plane. The power distribution model can be partitioned on an individual device basis since the components are distributed over the PCB.



Power-Ground Plane Construction
Figure 7

In the basic per device model, the plane inductance (L_p & L_g), parallel-plane capacitance (C_p), parallel-plane impedance (Z_p), and plane resistance (R_p & R_g) are:

$L_p = L_g = 0.032 \bullet t/W$ nH/in 5)

$R_p = R_g = R_t \bullet N$ Ω 6)

$Z_p = 0.377 \bullet t / (W \bullet \sqrt{\varepsilon_r})$ Ω 7)

$C_p = 225 \bullet \varepsilon_r \bullet A/t$ pf 8)

Where,

R_t = Power plane resistivity (ohms/square)
N = Number of squares
A = Surface area (square inches)
t = Plane separation (mils)
W = Conductor width (inches)

The plane inductance and impedance should be calculated using a finite-element model or discretely as AC current does flow between IC's and nearby decoupling capacitance.

Current provided by a plane acts as a distributed capacitor since it is connected directly to the device power leads. SANMINA's BC-2000 material provides approximately 506 pf/in^2 capacitance as supplied to the PCB fabricator. The net capacitance is less than this once the via clearance pads are calculated, since they remove copper from each of the planes. A general equation presenting net capacitance is:

$$C_{Net} = 506 \bullet (Area_{Plane} - Area_{Via}) \text{ pf} \qquad 9)$$

Where, C_{net} = Net Plane Capacitance (pf)
$Area_{Plane}$ = Initial Plane Area (in^2)
$Area_{Via}$ = Clearance Pad Area (in^2)

Current is provided via a transmission line from the remote capacitors if the nearest capacitance is depleted and if current has not been depleted from that remote area. If the plane is sub-divided into isolated areas the capacitance for each area will need to be calculated independently.

2.5.2 Switching Transient Capacitance

Switching transient capacitance provides very fast energy to charge the output sections of the device during an output transition. This typically is the highest speed content of the waveform and requires the least energy. If insufficient energy is available, the signal transition time will degrade prior to leaving the device package.

In very high speed devices, the decoupling capacitance may be built into the package to minimize the lead inductance between the capacitance and the device. Typically, this energy is provided by the distributed plane capacitance (Buried Capacitance) or .01 F decoupling capacitors.

BC-2000 has demonstrated power plane peak noise reductions up to 1V. This provides a quieter/more stable power distribution grid. This also provides the ability to reduce the noise budget allocation for switching noise.

2.5.3 Line Charging Capacitance

Line charging capacitance provides switching current through the output stages to charge the signal line and attached loads. The charge current is required until the line reaches its quiescent state. If insufficient capacitance/current is provided, the edge transition time will degrade.

Two types of line charging capacitance are required: one for capacitive lines and one for transmission lines. Capacitive line charging requires a faster, high peak charging rate than a transmission line. A transmission line requires a slower, but typically longer pulse to keep the line charged until all of the reflections are over. The energy required for these demands are typically provided by the distributed plane capacitance (Buried Capacitance) or 0.01 - 0.1 F discrete decoupling capacitors.

2.5.4 Low Frequency Bulk Capacitance

Low frequency capacitance is often termed *bulk* capacitance. This capacitance is used to recharge power planes and higher frequency charging capacitors, and provide switching current for lower frequency requirements. The recharge current is provided during the primary clock interval and at lower frequencies which are established by architecturally set cycles. Capacitance values will range from 1 - 47 F.

2.6 Integrated Circuit Decoupling

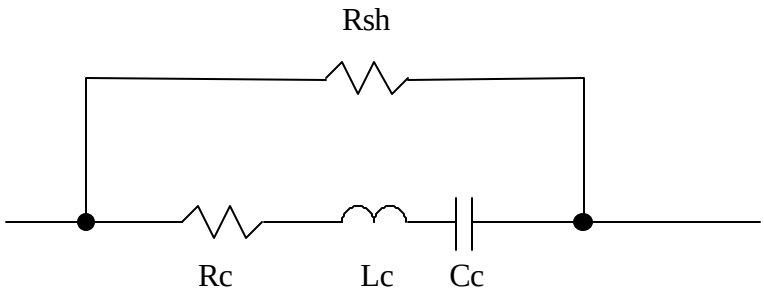
A printed circuit board power distribution system must provide sufficient current, in time, for the circuitry inside a mounted/packaged device to operate. This includes high peak current requirements during output switching. The power distribution system must provide this current without lowering the input supply voltage below its minimum acceptable threshold.

When the power supply is too far away or the stored energy in the board is insufficient, discrete capacitors are placed near the devices, connected between power and ground planes, to provide this current. In a sense, these capacitors provide the charge current to the device instead of the power planes. When they discharge their current into the device they quickly recharge from energy stored in slower discharging capacitors and power supplies prior to the next required discharge “request”.

The frequency response required by the decoupling capacitor system may be predicted by transposing the time domain waveform into its components using a Fourier Transform. As shown in prior sections the frequencies that must be provided are much higher than the system, or circuit, clock frequency. In order to minimize the signal edge rate degradation the current for the frequencies which compose the state change rise time must be provided. Typically, current must be provided for frequencies 10 to 100 times higher than the primary clock frequency.

2.7 Capacitor Model

The lumped constant equivalent circuit of the capacitor is illustrated in Figure 8. R_{sh} is the insulation resistance and typically has a value >100 MΩ and is generally omitted. It has a minimal effect on the operation of the capacitor and will be omitted from further discussions. R_c is the series resistance. L_c is composed of lead and plate inductance. C_c is the bulk capacitance.



Lumped Element Capacitor Model
Figure 8

The total effective impedance, Z_c of the capacitor is:

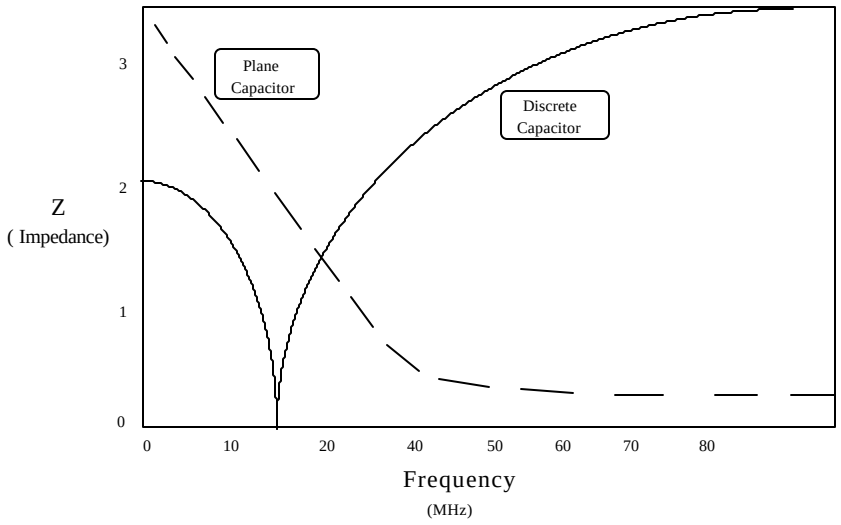
$$Z_C = SQRT(R_C^2 + (X_L - X_C)^2) \quad \Omega \quad 10)$$

where, R_C = Series lead and plate resistance Ω

$$X_L = 2 \bullet \pi \bullet f \bullet Lc \quad \Omega \quad 11)$$

$$X_C = 1/(2 \bullet \pi \bullet f \bullet Cc) \quad \Omega \quad 12)$$

The series inductance and capacitance yield a resonant frequency at which the effective impedance will equal the series lead resistance, R_C. Below resonance Z_C is dominated by the capacitive reactance. Above resonance Z_C is primarily inductive reactance. Decoupling capacitors only provide current below resonance. The peak current is provided at the resonance point. Typically, higher value capacitors have lower resonant frequencies due to larger plate and lead inductance resonating with the larger capacitance.



Plane and Discrete Impedance
Figure 9

2.8 Decoupling Capacitor Operation Summary

Ideally the power distribution system should be a zero resistance system identical to and parallel to the ground distribution system. However, even in an ideal power/ground system there is still a problem that will occur on the power supply lead. This problem is caused by the *parasitic* inductance present on the power lead, which produces a voltage differential or *sag* governed by $Vs = L \Delta I / \Delta t$. The common method of dealing with this is to employ a capacitor connected between power and ground supply leads to bypass this voltage sag or *noise.*

Typical values for these types of capacitors are 0.1 f, 0.01 f, 0.001 f, etc. These types of capacitors are available in a variety of packages for surface mount assembly. Since it is known that the leads of this bypass capacitor will possess the electrical components of resistance and inductance the discrete bypass capacitor is a series resonant circuit with a specific resonant frequency. This resonant frequency must be matched to the frequency of the noise to be bypassed or the decoupling will not be effective.

A more effective method of dealing with this problem (especially at higher frequencies) is to employ a *distributed plane capacitance* to decouple the power supply. A distributed plane has very low transmission line inductance coupled with a very fast recharging capacitance. This combination makes this system ideal for rise times of 2 ns or less, which is the break point of effectiveness between discrete surface and distributed internal systems.

3.0 EMI / EMC Control

Buried Capacitance lowers the power distribution impedance by increasing the capacitance and lower the inductance of the power planes. The actual effect will vary dependent on the application.

3.1 EMI Avoidance

Most EMI problems are created when high frequency current transients generate significant RF potentials on the power plane due to lead inductance. The instantaneous short circuit current created during a low-high output transition creates a momentary current short on the power plane and creates high frequency "noise" in the system. This noise can be easily coupled to the external device through I/O cables and PCB traces. The other sources of EMI problems are from the unterminated ground loop creates a broadband problem and from unshielded cables that serves as a radiation antenna.

The following list presents areas to be considered from an EMC design perspective:

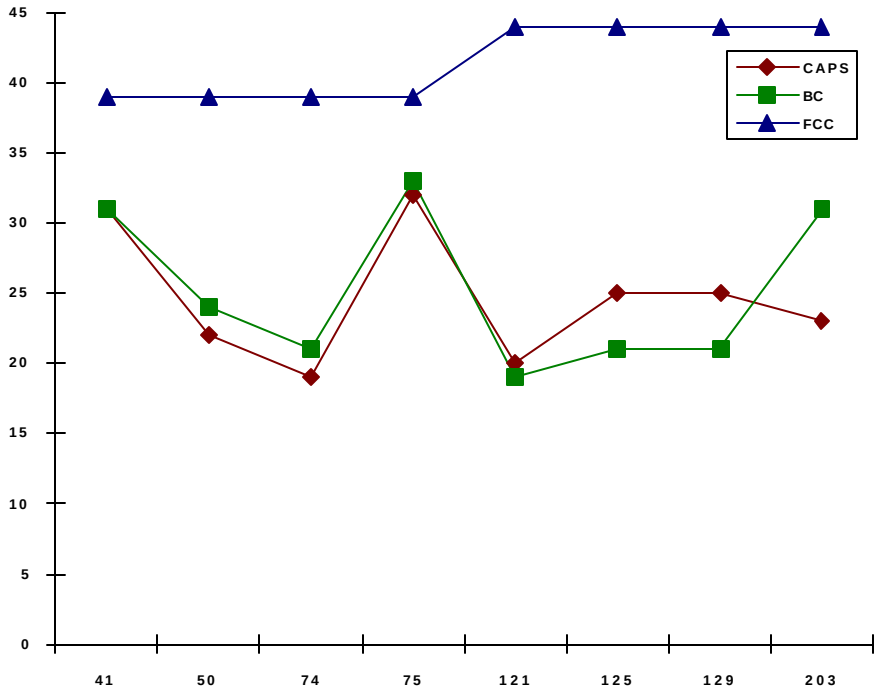
- Select good shielding case for the system
- Choose low EMI components
- Use distributed capacitance to dampen high frequencies
- Use discrete bypass capacitance to dampen lower frequencies
- Reserve space for EMI filters
- Keep clock traces short and apart to avoid crosstalk
- Provide low impedance ground to terminate noise
- Use shielded I/O cables with good continuous ground connections

3.2 Buried and Discrete Capacitance Utilization

Buried and discrete capacitance can be utilized to reduce EMI below required emission levels. Effective use of BC reduces the need for discrete capacitors.

A Buried Capacitance board has internal capacitance of approximately 506 pf/in^2 per layer pair. For example, the theoretical capacitance for a 100 square inch board with two capacitance layers will be 0.1μf. The net total capacitance for the board will be 10 to 20% less than the maximum value because of copper that is removed for via hole anti-pads and etching borders associated with the power and ground planes.

Some boards have a mixture of digital and analog components. They require separate power and ground planes for EMI purposes or for isolation of different operational voltages on the digital and analog planes. In this case, the discontinuation of power or ground plane will result even less net capacitance in the board. To compensate for this some 1μf and 0.1μf bypass capacitors will have to be incorporated.



Example Board Assembly Radiated EMI Plots With and Without BC
Figure 10

Generally, for electronic designs IC's fire sequentially or randomly BC should provide sufficient capacitance for the system. However, by incorporating all of the original bypass capacitors into the system will result more EMI problems. Here is the explanation.

The buried capacitance material is imaged using existing power and ground layers and it is laminated as an integral part of the circuit board. By sharing capacitance, it provides sufficient, instantaneous distributed capacitance with minimum inductance. Theoretically, with additional unnecessary discrete bypass capacitors, it will consume more energy and hence will increase the internal current flow. The increasing current flow and additional inductance from the discrete bypass capacitors will induce more noise into the system creating more EMI. This is why it is a common misconception that adding more capacitors to the board will result quieter emissions.

If these general guidelines are inconclusive, it may be better to manufacture two board configurations. The first board should be populated with all discrete bypass capacitors. The second board should incorporate Buried Capacitance layers and be assembled without any discrete bypass capacitors. The same artwork can be utilized for both test boards. The EMI tests can then be conducted on both boards under the same conditions and have the results compared. The measurements will provide comparative data on how effective the Buried Capacitance performs versus the conventional method.

3.3 EMI Test Failure Analysis

The analysis of an assembled PCB to predict EMI generation and suppression is a complex subject. There are instances when the analytical tools are insufficient to provide a correct solution and testing must be performed. Prior to utilizing BC as a solution, a root cause analysis should be performed to isolate the cause(s). This section provides some general guidelines for approaching this analysis.

3.3.1 Problem Identification

The first step to take when the Equipment Under Test (EUT) fails to comply with FCC/VDE limits is to locate the source of the problem. To determine the problem, first move the system to the maximum radiation position. Then remove all the external devices one at a time and observe any changes from the spectrum analyzer. If there is any changes from the spectrum analyzer, this indicates the problem is from the external device or the results of the combination of both the EUT and the external device. The mismatch impedance, unshielded wire or poor grounding connections can cause EMI problems.

If all the connected ports are removed from the EUT and the emission reading remains the same, inspect any shielding leakage that is occurring from the system. Generally, most digital and electronic design will require system shielding. Shielding of all external cables will also be required to minimize radiated emissions. The chassis for the system mostly use metal or plastic coated with conductive material. After inspecting the system using the above steps, the remaining problems will be the system design or internal connection problems.

3.3.2. Input/Output Related Problems

Most Input/Output (I/O) problems result from poor grounding or mismatched load impedance. The solution for these problems may involve shielding, decoupling and/or filtering. When shielding the transmission line, make sure the shielding material is connected to the chassis ground versus the signal ground plane. Another solution is by adding bypass capacitance to data and clock signal traces to terminate the signal being emitted onto the drain into the external device and to reduce the high frequency components.

However, connecting the discrete decoupling capacitors to traces on the PC board may make matters even worse. We do not want to decouple a signal ground. We need to bypass a physical location that doesn't vary with respect to earth ground. The location of the bypass capacitors must be as close to the output port(s) as possible. But, these bypass capacitors may contribute some propagation delay into the circuitry. Normal electrical design criteria will indicate what capacitor value and dielectric will be appropriate for the system.

3.3.3. Low Frequency Problems

Frequencies below 200Mhz are considered as low frequency. Most of the low frequency problems cannot be solved by using shielding techniques. Most low frequency problems are created by poor grounding, poor layout, crosstalk or a lack of efficient bypass capacitance in the system. As was mentioned before, if the board provides insufficient area to generate enough buried (distributed) capacitance for the system or a significant quantity of components fire simultaneously, a few of the

discrete bypass capacitors will be required to assist the buried capacitance. The capacitors should be located evenly throughout the board.

The best practice is to mount the bypass capacitors evenly between the IC's VCC and ground connections. In addition, you can use the following techniques to assist in solving remaining problems:

- Improve the grounding on the system board by adding more grounding
- Change all the plastic stands to metal stands
- Add bypass capacitors to each quadrant of the board
- Add ferrite cord to the internal cables
- Control the signal wave form from the oscillator output to a smooth sine function waveform by adding ferrite beads for low frequency and resistors to dampen the high frequency components

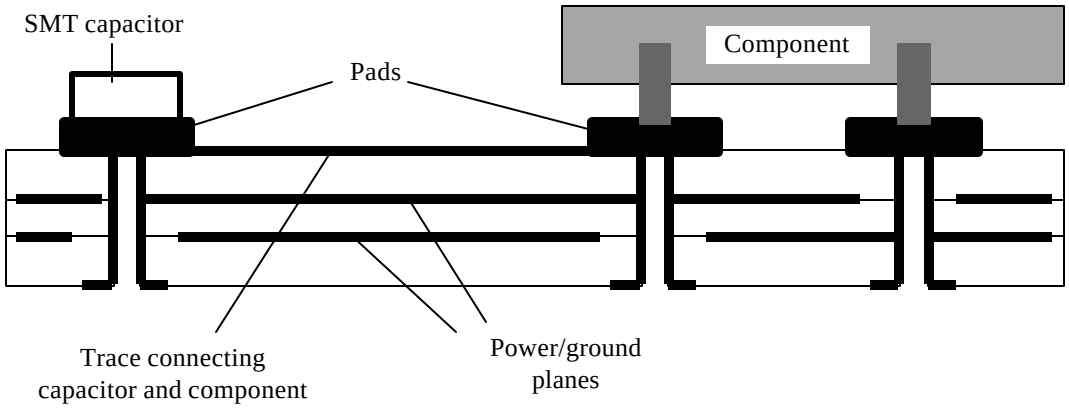
3.3.4. High Frequency Problems

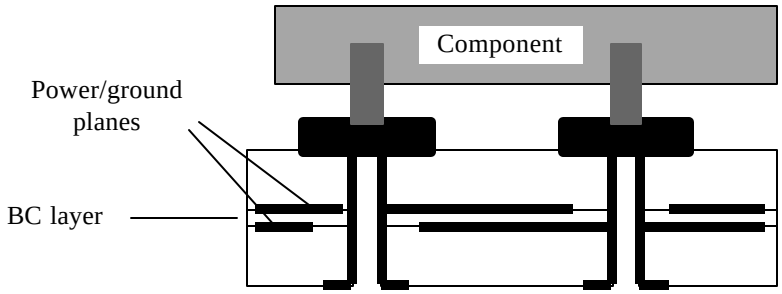
Shielding techniques can be used to solve emission problems at frequencies above 200 Mhz. First inspect the case where leakage may occur by squeezing the case from different angles and observing any changes on the spectrum analyzer. Once the gap has been located, use metal gaskets to shield the leakage. If the case is plastic material, conductive coating material may need to apply.

3.3.5. Buried versus Discrete Capacitance at High Frequencies

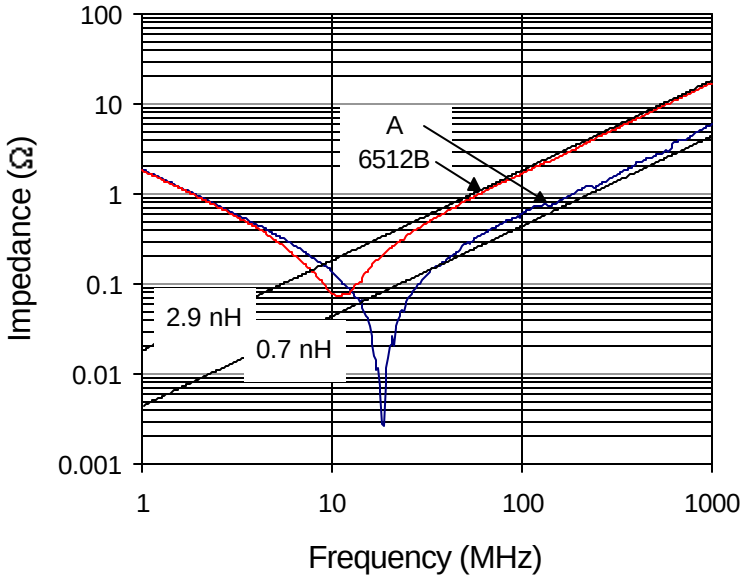
Buried capacitance is very effective when utilized to bypass the higher frequency components. BC has been used to reduce the EMI generation within the board, near the components, thus negating additional system level shielding requirements. The successful use of BC is mainly due to its low impedance performance observed at high frequencies.

To lower the EMI noise, the impedance of the power distribution system needs to be as low as possible. At high frequencies, this means the inductance of the system must be carefully controlled. A system using discrete capacitors will have inductance contributed from the power/ground planes, vias accessing the planes, pads for capacitor mounting, traces connecting capacitor to the component and the inherent inductance of the capacitors (Figure 11). The last two contributors to the inductance can be eliminated when switching to BC. Figure 12 shows the impedance measured from a mounted SMT capacitor versus a BC board. BC board presents significantly lower impedance at high frequencies.





Physical model of power distribution systems using discrete capacitors vs. BC
Figure 11

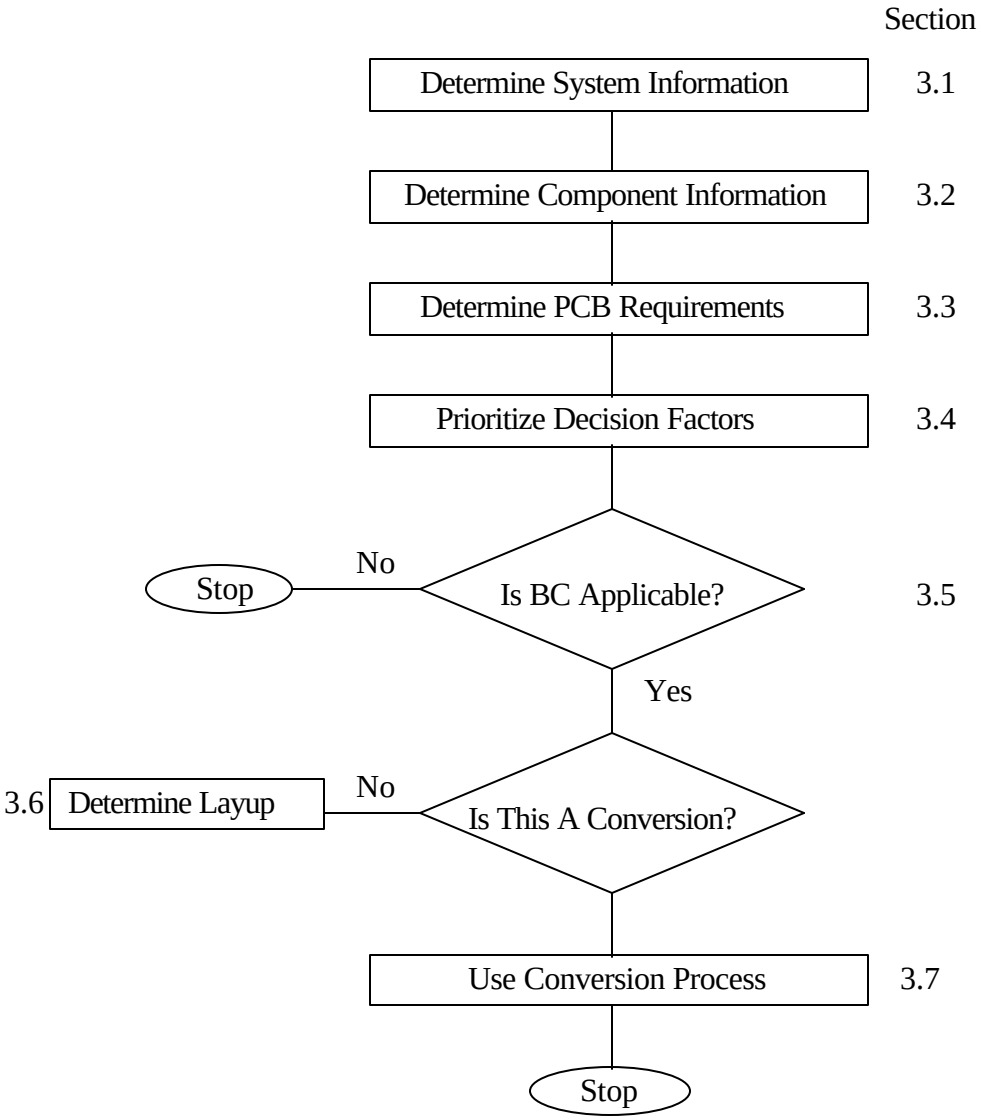


Impedance of a SMT capacitor (6512B) and a BC test board (A)
Figure 12

4.0 Buried Capacitance Design Techniques

Buried capacitance is very effective when utilized in proper applications. This section provides general guidelines, based on existing applications, on how and when to utilize BC within a PCB.

The decision tree presented in Figure 13 provides a general process for using BC. More detailed information is provided in the following subsections. The form which is used with this decision tree is in section 4.1. Appendix A.3 has an additional form which can be used for copying.



Buried Capacitance Design Decision Tree
Figure 13

4.1 System Information

- **Functionality:** Buried Capacitance primarily provides high frequency switching current enhancement for power planes. Typically digital versus analog devices will utilize this current. In cases of mixed technology PCB's the BC area in the analog sections can be utilized for the digital circuitry decoupling.
- **Digital Device Technology:** The device technology that is utilized determines the base edge switching rates. This establishes the frequency content the BC layer must provide current to. EMI performance is also dependent on the frequency content. To some extent, the device technology is also a key driver in the system primary clock frequency selections.
- **Component Packaging:** Through-hole packages require large plated through holes and have long package leads. The large holes will remove available copper on the BC layers which create the capacitor plates. They also create larger discontinuities between the power system and the IC die. Surface mount or direct die attach packaging will maximize the BC performance.
- **Component Mounting:** PCB's which currently do not utilize BC and have a low quantity of components on the secondary or solder side may be able to move the secondary components to the primary side after the BC conversion.
- **Primary Clock Frequencies:** The high frequency current that is provided by BC is generally significant for systems with clock frequencies between 30 and 100 Mhz. Systems which have a primary clock frequency below 30 Mhz will require additional capacitance which can be provided by discrete capacitors. Systems with clock frequencies above 100 Mhz require custom analysis due to the heavy losses introduced by the high frequency dissipation characteristics of FR-4 material.
- **Device Switching Edge Rates:** Signal edge switching rates between 1 to 10 ns will generally draw a significant amount of their current from the BC layers. Edges less than 1 ns will be affected due to the high dissipation characteristics of FR-4. Edge rates greater than 10 ns require more current than BC can provide and will require discrete capacitors.
- **Safety Compliance:** BC is approved by Underwriters Laboratories V-0 flammability rating (UL File # E62273).
- **EMI Class:** Designs may be able to reduce additional components and shielding by utilizing the BC layers to reduce the high frequency signal levels which will increase the radiated emissions. BC has demonstrated the ability to provide from 3 - 10 dB radiated noise reduction in the 30 - 200 Mhz spectrum.
- **Operating Temperature Range:** BC is specified as a commercial or industrial grade material. It's operating temperature range, as approved by UL, is -40 to +85°C.
- **System Power Voltages:** Each voltage plane can be substituted with BC to enhance performance, independent of other plane interference's. Planes which have multiple voltages, or split planes, must divide the capacitance into separate capacitors.

4.2 Component Information

- **Random Logic IC's:** Random logic IC's generally have a significant amount of asynchronous data switching. These components will utilize BC properties very effectively.

- **Bus Interface IC's:** These devices generally have a large switching current due to very large output driver structures and large capacitive or transmission line loading. These devices require a large amount of high speed current which is larger than BC layers can provide. Additional discrete decoupling capacitors will be required.
- **Memory IC's:** Memory IC's generally are assembled in synchronous arrays. When these arrays are clocked, a large amount of switching current is required to drive the output interfaces and charge the internal memory array's. These devices require a large amount of high speed current which is larger than BC layers can provide. Additional discrete decoupling capacitors will be required.
- **Decoupling Capacitors:** For applications where BC is being utilized to reduce or eliminate discrete capacitors, the actual value and frequency response of the capacitor must be identified. Generally, BC can replace decoupling capacitors in the range of 0.001 to 0.01 μF.

4.3 PCB Requirements

- **Size:** The X-axis, Y-axis and thickness is required, as one of the parameters, to determine the layer configuration (layup) possibilities. It is also used to determine the amount of available capacitance for capacitor substitution applications.
- **Useable Area:** This is utilized to determine the amount of net available capacitance. This is utilized as the basis prior to subtracting via clearance pads to determine the actual capacitance of the board.
- **Material:** BC-2000 material is FR-4 and must be compatible with the other materials utilized in the board. The BC fabricator can provide compatibility information.
- **Layup:** The layup that is required for the final board is selected from the table at the end of the evaluation form. Section 4.6 of this document also provides guidelines for selecting the appropriate BC based layup.
- **Quantity of Split Power Planes/Size:** Since each split power plane in effect creates separate capacitors, the size of the planes is required. This will determine the basis for the capacitance calculation for each voltage. If there is in-sufficient capacitance with a single BC layer pair, more layers may be added to achieve the required capacity.
- **Nominal Signal Trace Widths:** This information is required by the PCB fabricator as one of the parameters to establish the quantity of layers that may be fabricated. This will be provided by the fabricator.
- **Signal Impedance:** Each of the signal layer impedance should be indicated on the layup drawing. This is utilized by the fabricator to establish the PCB construction. The PCB should have the copper layers evenly distributed through the board Z-axis to negate warpage. Offset layers can be fabricated on an exception basis to ensure that the electrical properties of the signals are achieved.

4.4 Rate Decision Factors

The decision factor rating is essential to ensure that the product goals are achieved. Since BC can be utilized in a multitude of applications it is important to understand what the primary intent is. Section 2 and 3 presented information on how BC can be

utilized for power distribution decoupling and EMI suppression. Section 6 presents non-performance areas where BC is applied.

4.5 Buried Capacitance Applicability

Based on the information provided from steps 1-4 a decision is made on whether BC is appropriate for the design under consideration. Due to the complexity of each design and the properties of BC an analytically exact analysis may not be possible. In this case, a test board should be fabricated and a “before and after” analysis must be made at both the board and system level. The results from this test can be maintained and utilized for future decisions on products within that, or similar, systems.

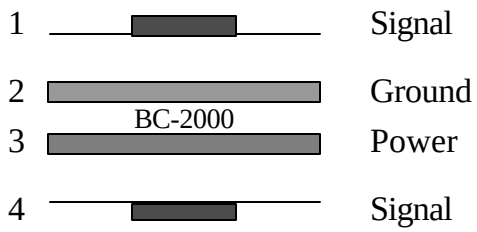
4.6 Determine Layup

The following PCB layer configurations, termed layups, are provided as a guide to select the most commonly utilized structures. These structures utilize commonly accepted manufacturing standards. Layer configurations other than these can be used, but should have PCB fabricator engineering input prior to use. The layer separation distances are not included because they will be established for signal performance and/or manufacturability/cost reasons.

The BC layers which utilize BC-2000 material have two 1 oz. (1.4 mil thick) copper layers which are separated by a 2.0 mil FR-4 dielectric. One copper layer is the power plane and the opposing layer is the ground plane.

4.6.1 Four Layer BC Layup

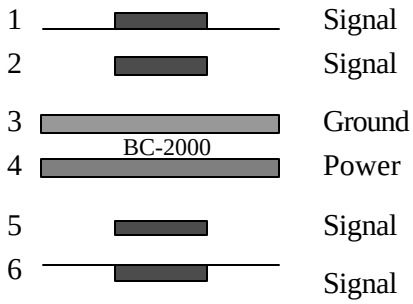
The following layup presents how BC-2000 can be utilized in a four layer PCB.



Four Layer BC Layup
Figure 14

4.6.2 Six Layer BC Layup

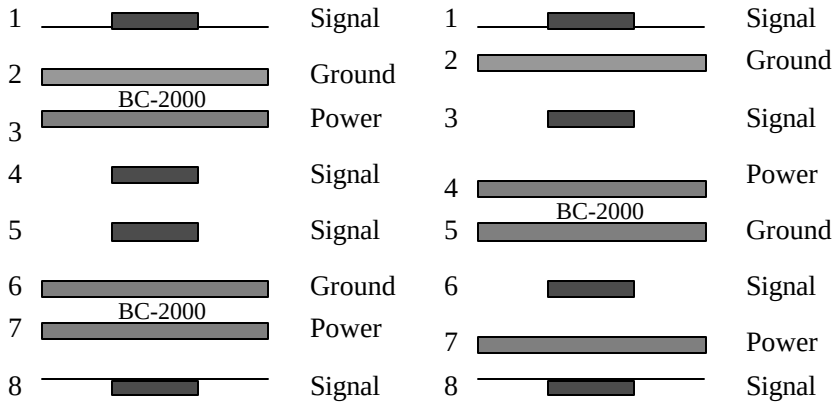
The following layup presents how BC-2000 can be utilized in a six layer PCB.



Six Layer BC Layup
Figure 15

4.6.3 Eight Layer BC Layup

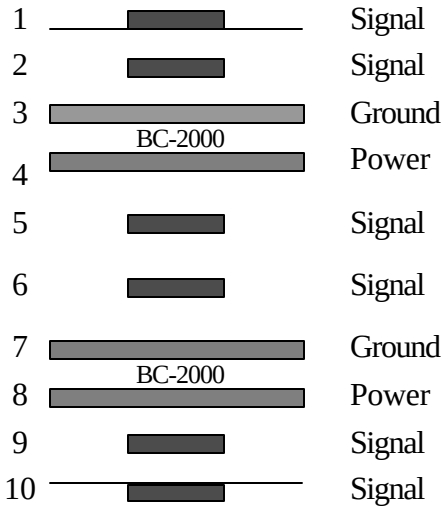
The following layup presents how BC-2000 can be utilized in an eight layer PCB.



Eight Layer BC Layup
Figure 16

4.6.4 Ten Layer BC Layup

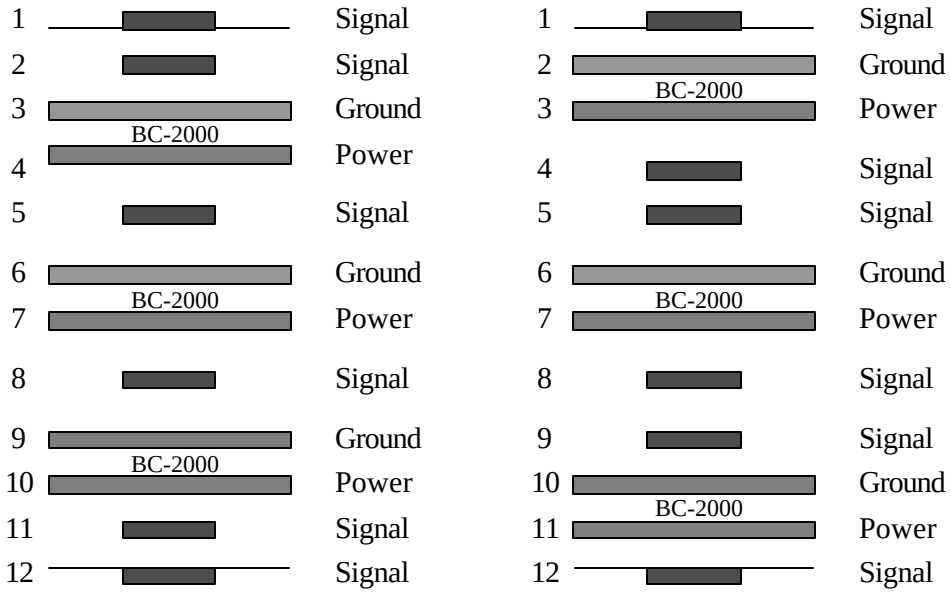
The following layup presents how BC-2000 can be utilized in a ten layer PCB.



Ten Layer BC Layup
Figure 17

4.6.5 Twelve Layer BC Layup

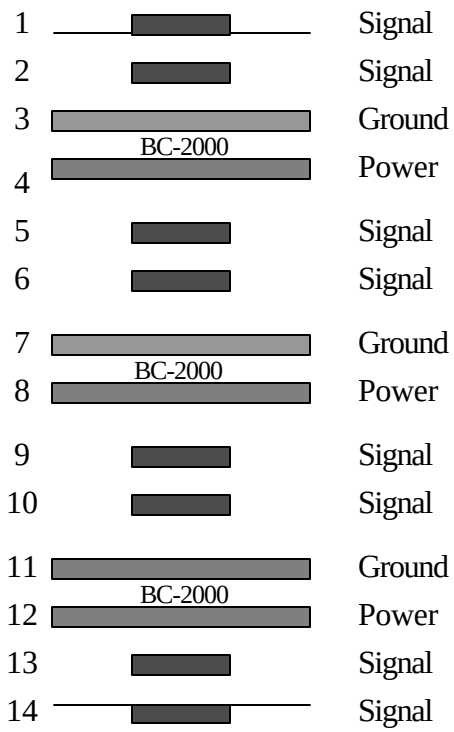
The following layup presents how BC-2000 can be utilized in a twelve layer PCB.



Twelve Layer BC Layups
Figure 18

4.6.6 Fourteen Layer BC Layup

The following layup presents how BC-2000 can be utilized in a fourteen layer PCB.



Fourteen Layer BC Layup
Figure 19

4.7 Buried Capacitance Conversion Process

The following process describes a general process for converting a PCB design that currently does not utilize the BC technology to a PCB which incorporates BC-2000.

Step

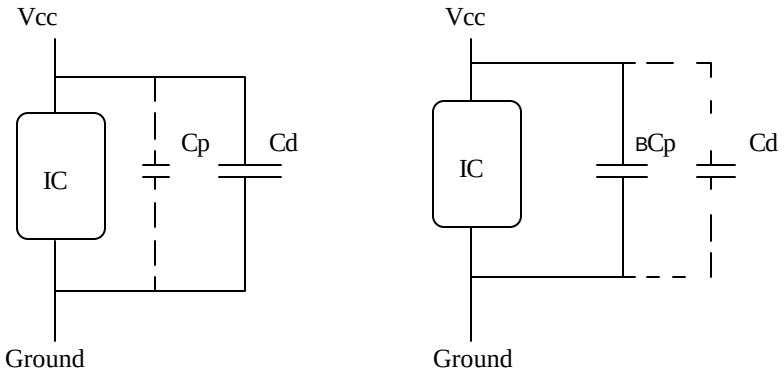
1. Complete the Buried Capacitance Evaluation Form, appendix A.3, for this application. This step is especially important for initial product applications, as it provides concise engineering data to help define the proper course of action.
2. Use the existing artwork, including the existing power and ground layers to construct the Buried Capacitance PCB. The following general guidelines may be used to convert a standard PCB:

- Substitute a BC-2000 sandwich for each power or ground layer in the existing PCB. Section 4.6 provides guidelines for this.
- Etch power and ground on opposite sides of the BC-2000 layer.
- Ground layers should be positioned to face " hot " clock lines if possible.
- If the clock lines are unknown, then ground should face layer 1.
- Impedance control layup will have to be adjusted (normally a simple matter)

3. Fabricate the new PCB prototype.
4. Assemble and test the prototype. It is recommended that all components including bulk capacitors be assembled onto the PCB, with the exception that *no*

bypass capacitors be mounted at this time. Measurements of power/ground noise and radiated EMI can then be compared to the existing non-capacitive PCB. If for any reason it is determined that additional bypassing is required, then it is recommended to only replace a *minimum number* of surface capacitors, starting with the largest value first.

5. After a determination has been made of the number of capacitors that can be removed from the surface of the PCB , those capacitor positions are removed from the CAD file of required parts and the PCB may be reploted. At this time the designer may choose to review options created by the removal of those capacitors and the associated conductors, pads and via holes that supported them. (*Note: Generally CAD systems that have performed redesigns removing capacitors complete this step automatically after the instruction to remove the capacitor has been given. This is a simple step due to the fact that the original bypass capacitor was connected in parallel with the active device, refer to Figure 20.)* Typically new components may be added, the board size may be reduced or components may all be moved to one side.



Standard PCB

Cd= Large Discrete Capacitor

Cp= Small Plane Capacitance

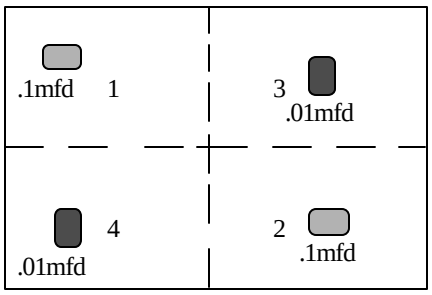
Buried Capacitance PCB

BCp=Large Plane Capacitance

Cd= Discrete May be Added If Desired (in very small quanities)

Standard and BC Capacitor Configuration
Figure 20

6. It is recommended that all components including bulk capacitors be assembled onto the PCB, with the exception that *no bypass capacitors be mounted at this time.* Measurements of power/ground noise and radiated EMI can then be compared to the existing non-capacitive PCB. If for any reason it is determined that additional bypassing is required, then it is recommended to only replace a *minimum number* of surface capacitors, starting with the largest value first.



Capacitors of correct value should be added in pairs 1,2 and 3,4 in opposit quadrants of the PCB. This suggestion also applies to individual planes s as split power planes or isolated islands.

Power Plane Discrete Capacitor Placement
Figure 21

4.8 General Use Guidelines

It has been demonstrated in several designs and verified by testing that the effective use of distributed capacitance can be determined if the following parameters are within the following equation:

$$R_t \bullet I_{tr} \div A \leq 5 \qquad 13)$$

Where, R_t = Rise time of the primary digital clock pulses (ns)
A = Area of the undivided plane (in^2)
I_{tr} = Peak device current (ma)

Distributed capacitance is a very fast acting and quick recharging capacitor. For this reason it is recommended for high frequency (30 Mhz and faster) digital applications, and it is not recommended for memory boards or boards in which bus drivers constitute a significant percentage of the total components. This of course is only a general guideline because of the many other variables in each printed circuit design.

5.0 Buried Capacitor Technical Specifications

5.1 Materials Requirements

5.1.1 Reference Documents

- IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits
- IPC-L-108 Specification for Thin Metal Clad Base Material for Multilayer Printed Boards
- IPC-L-109 Specification for Resin Preimpregnated Fabric (Prepreg) for Multilayer Printed Boards
- IPC-FC-241 Flexible Metal-Clad Dielectrics for use in Fabrication of Flexible Printed Wiring
- IPC-FC-231 Flexible Bare Dielectrics for use in Flexible Printed Wiring
- IPC-FC-233 Flexible Adhesive Bonding Films
- IPC-MF-150 Metal Foil for Printed Wiring Boards
- IPC-RB-276 Qualification and Performance Specification for Rigid Printed Boards
- IPC-RF-245 Printed Qualification and Performance Specification for Rigid-Flex Boards
- J-STD-003 Solderability Test Method for Printed Wiring Boards
- IPC-TM-650 Test Methods Manual
- MIL-S-13949 Boards), Plastic Sheet, Laminated , Metal Clad (for Printed Wiring General Specification for
- TR-NWT-000078 Generic Physical Design Requirements for Telecommunications Products and Equipment
- UL 94 and Tests for Flammability of Plastic Materials for Parts in Devices Appliances

5.1.2 Definitions

All terms used in this document are defined according to IPC-T-50. The following terms are used as a supplement to IPC-T-50.

- Rigid Base Material: Base material that is reinforced by fiber or particulate and has a tensile modulus higher than 2500 ksi.
- Flexible Base Material: Base material that has a tensile modulus less than 2500 ksi.
- Comparable Base Material: New developmental materials are not likely to be included in the IPC or MIL specifications. In this case, the specifications of a comparable base material may be used for evaluation purpose. This comparable base material shall be determined by the R&D Department based on the various material properties (electrical, mechanical, chemical, thermal, etc.).

5.2 Base Materials Specifications

5.2.1 General Specification for Rigid Base Materials

Materials fall into this category shall comply to the specification listed in IPC-L-108, for the applicable resin systems. Base materials that are not classified in this specification shall at least meet the requirements of FR-4 or a comparable base material. Some of the required properties are listed in Table 1.

5.2.2 General Specification for Flexible Base Materials

Materials fall into this category shall comply to the specification listed in IPC-FC-241, Class 3 for the applicable resin systems. Base materials that are not classified in this specification shall at least meet the requirements of a comparable base material described in IPC-FC-241. Some of the required properties are listed in Table 1.

5.2.3 Special Requirements for Ultra-thin Base Materials

5.2.3.1 Thickness Tolerance

The thickness tolerance is ± 10% with a Cpk = 2.0, unless specified otherwise.

5.2.3.2 Copper Foil

All copper foil used on double sided clad laminates shall be designated as CFE31D and meet or exceed the minimum mechanical properties defined by “Type 3”, or commonly referred to as “High Temperature Elongation” (HTE), copper described in IPC-MF-150.

5.2.3.3 Glass Transition Temperature

Base materials shall have a minimum glass transition temperature (T_g) of 135°C.

5.2.3.4 Moisture and Insulation (Electromigration) Resistance

Under the test conditions specified in TR-NWT-000078 (85°C, 85% RH, 10 VDC bias for 500 hours, test under 45 to 100 VDC), the initial insulation resistance shall be less than 10 times the final insulation resistance. The Bellcore test uses the comb pattern to test the insulation resistance between the traces on the same plane. It is more applicable to measure the insulation resistance between the power and ground planes for the BC material. Therefore, the test shall be performed over a 12” x 12” area across the thickness of the base material. The larger the area that is sampled the higher the probability we will find a “weak” spot that may have electromigration problem.

5.2.3.5 Insulation Resistance

Similar to the reason described in 5.2.3.4, a 12" x 12" coupon shall be used to test the insulation resistance between the power and ground planes. The test condition is per TR-NWT-000078 (35°C, 90% RH for 4 days, test under 45 to 100 VDC). The minimum resistance is 500 megohms.

5.2.3.6 Chemical Resistance

Under the test conditions specified in IPC-TM-650, 2.3.2, the measured peel strength shall meet the minimum requirements defined in IPC-L-108 for rigid base material.

5.2.3.7 Moisture Absorption

Base material shall meet the maximum moisture absorption specified in IPC-FC-241. Rigid base materials shall use the criteria in IPC-FC-241 for the corresponding resin systems.

5.2.3.8 Capacitance Measurement

Base material shall provide a minimum of 506 pF/in^2 of capacitance, when measured with a LCR meter at 1 kHz.

5.2.3.9 Flammability

Base material shall be UL 94-V0 approved.

5.2.3 Test Method Specifications

Refer to IPC-L-108, IPC-FC-241, MIL-S-13949 and IPC-TM-650 for the details of the test methods and conditions. The test methods associated with some of the key requirements are listed in Table 1.

	Properties To Be Tested	Test Methods IPC-TM-650 unless specified otherwise	
		IPC-L-108	IPC-FC-241
1	Peel Strength	2.4.8.	2.4.9.
2	Volume Resistivity	2.5.17.	2.5.17.
3	Surface Resistivity	2.5.17.	2.5.17.
4	Dielectric Constant	MIL-S-13949	2.5.5.3.
5	Dissipation Factor	MIL-S-13949	2.5.5.3.
6	Flammability	UL 94*	UL 94*
7	Dimensional Stability	2.2.4.	2.2.4.
8	Thermal Expansion (Z)	2.4.41.	
9	Glass Transition Temperature	2.4.24.	2.4.24.*
10	Chemical Resistance	2.3.2.*	2.3.2.
11	Electrical Strength	2.5.6.	ASTM D-149
12	Arc Resistance	2.5.1.	
13	Solder Float	IPC-L-108 4.6.24.	2.4.13.
14	Thickness Tolerance	± 10 %*	± 10 %*
15	Surface Finish of Cu Foil	2.4.15.	
16	Tensile Strength		2.4.19.
17	Elongation		2.4.19.
18	Initiation Tear Strength		2.4.16.
19	Propagation Tear Strength		2.4.17.1.
20	Fatigue Ductility		2.4.3.2.
21	Flexural Endurance		2.4.3.
22	Low Temperature Flexibility		2.6.18.
23	Density		ASTM D-792
24	Solderability		J-STD-003
25	Insulation Resistance	Bellcore TR-NWT-78*	BellcoreTR-NWT-78
26	Moisture/Insulation Resistance	Bellcore TR-NWT-78*	BellcoreTR-NWT-78
27	Moisture Absorption	2.6.2.*	2.6.2.
28	Capacitance Measurement	**	**
29	Fungus Resistance	2.6.1.	2.6.1.

Properties to be tested and the associated test methods for base materials
Table 1

* Indicates that the property to be tested is either not required by the IPC specification or the test method is deviated from the original IPC specifications.

** Capacitance measurements shall be performed by using a LCR meter with an accuracy of ± 3% or better.

5.3 Fabricated PWB Specifications

In this particular application the Buried Capacitance™ layer is completely embedded in the PWB. The characteristics of the finished PWB do not fall into the classification of a rigid-flex PWB even if a flexible base material were used. (Both Type A and B require the capability to withstand some degree of flexing.) Consequently, all fabricated PWB's shall comply to the IPC-RB-276, Class 3 requirements. The only exception is that no minimum dielectric thickness is required. Some of the test items are listed in Table 2.

	Test Items	Paragraph in IPC-RB-276
1	Material	3.5
2	Visual	3.6
3	Soderability	3.6.5
4	Surface	
5	Hole	
6	Dimensional	3.7
7	Physical	
8	Plating Adhesion	3.6.6
9	Bond Strength	3.10.3
10	Construction Integrity	
11	PTH Integrity Prior to Stress	3.9.1
12	Additional Dimensions	3.9.2
13	PTH After Stress	3.1
14	Thermal Stress (solder float)	3.10.1
15	Rework Simulation	3.10.2
16	Electrical Requirement	3.12
17	Dielectric Withstanding Voltage	3.12.1
18	Circuit Continuity	3.12.2.1
19	Isolation	3.12.2.2
20	Short to Metal Substrates	3.12.3
21	Insulation Resistance	3.12.4
22	Environmental	3.13
23	Thermal Shock	3.13.2
24	Cleanliness, Ionic	3.13.3.1
25	Special Requirements	3.14
26	Outgassing	3.14.1
27	Cleanliness, Organic	3.14.2
28	Fungus Resistance	3.14.3
29	Vibration	3.14.4
30	Mechanical Shock	3.14.5
31	Impedance Testing	3.14.6
32	Thermal Expansion	3.14.7

Qualification tests for IPC-RB-276
Table 2

6.0 Additional Buried Capacitance Benefits

Buried Capacitance provides additional benefits beyond just performance and EMC enhancements. It can be utilized to reduce the assembled product cost, increase manufacturing quality, increase long term reliability and reduce the PCB size.

6.1 Cost Minimization

6.1.1 Manufacturing Placement Cost

Manufacturing costs can be reduced when BC is utilized to reduce the quantity of decoupling capacitors. An example calculation follows:

$$T_{PLACEMENT} = T_{MACHINE,CYCLE} + T_{SETUP}/N_{REEL} \quad 14)$$

$$COST_{PLACEMENT} = T_{PLACEMENT} * RATE \quad 15)$$

$$\Delta COST = COST_{PLACEMENT} * N_{CAPS} \quad 16)$$

Where, $T_{PLACEMENT}$ = Placement Time (sec)

$T_{MACHINE,CYCLE}$ = Placement Cycle Time (sec)
T_{SETUP} = Setup Time (sec)
N_{REEL} = Reel Part Quantity
RATE = Burdened Machine Rate ($)
N_{CAPS} = Quantity of Capacitors

6.1.2 Manufactured Cost Reduction

The total manufactured cost reduction that can be realized with BC combines the component procurement cost, manufacturing cost and overhead burdening. The following calculation can be utilized to determine to cost savings:

$$\Delta COST = (COST_{PLACEMENT} + COST_{MATERIAL} * COST_{BURDEN\_RATE}) * N_{CAPS} \quad 17)$$

Where, $COST_{MATERIAL}$ = Capacitor Purchase Price
$COST_{MATERIAL}$ = Factory Overhead Burden Multiplier

6.2 Quality and Reliability Enhancement

6.2.1 Defect per Unit (DPU)

The Defect per Unit (DPU) will be decreased when BC is substituted for discrete capacitors. There will be two less solder joints and possibly two less via holes per capacitor.

6.2.2 Mean Time Between Failure (MTBF)

The Mean Time Between Failure (MTBF) of the assembled product will be increased as decoupling capacitors are substituted with BC. The actual MTBF values can be obtained from DoD MIL-HDBK-217 or Bellcore FR-NWT-000978. These handbooks contain the MTBF calculation methodologies and the predicted values for the components.

6.3 PCB Design Simplification

6.3.1 Space Savings

As decoupling capacitors are removed from the primary and secondary sides of the PCB it can be made smaller or provide additional signal routing area. When determining space savings the area saved will be on the component mounting surfaces and all layers where the connection Vias pass through. The actual space savings is dependent on the package style and mounting land pattern that is utilized.

6.3.2 Routing Considerations/Elimination of Vias and Traces

The signal via and component land pattern reduction will provide additional PCB routing area on all layers. When a substantial quantity of devices are removed from the PCB and substituted with BC it may be possible to reduce the board size and/or reduce the routing layer quantity. Trace distances will also be reduced due to tighter component placement.

Another consideration when analyzing the real estate gain is that the assembly may be converted from a double-sided surface mount assembly to a single-sided mixed technology assembly. Many conventional SMT assemblies have the active components on the primary side and the passive decoupling capacitors on the secondary side. When the high frequency decoupling capacitors are removed it may be possible to only have components mounted on the primary side.

6.3.3 Quick Design Modification

During designer testing boards often run into performance and/or regulatory obstacles. Time is of the essence and BC has demonstrated the ability to correct problems in a timely manner.

By the movement of internal planes to create BC power/ground pairs poor or marginal high frequency performance can be enhanced without any artwork modifications. Each power and ground plane can be substituted with a BC-2000 core using the existing artwork.

EMC emission problems can also be corrected by adding BC-2000 cores. This lowers high frequency noise that is distributed across the PCB. 3 to 10 dBA of additional radiated emission attenuation has been demonstrated in system designs.

6.3.4 Design Cycle Reduction

The design cycle will also be slightly reduced. This is due to a shorter schematic capture and CAD PCB layout time reduction due to less components (discrete

capacitors) requiring to be entered into the schematic and laid out on the PCB. Component placement time can also be reduced since more surface area will available for other components.

A.0 Appendices

A.1 References

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A.2 Glossary

AEE:	Ambient Electromagnetic Environment levels of radiated and conducted signals and noise existing at a specified location and time. Atmospheric and man-made electromagnetic noise and signals, appearing over a wide spectrum, compose the "ambient environment". The ambient is almost always changing with time and the spectrum-amplitude profile may sometimes be better described statistically.
Ambient level:	The magnitude of radiated or conducted signals and noise existing at a specific test location and time with the equipment under test de-energized.
Anechoic enclosure:	A shielded enclosure whose internal walls have low reflection characteristics for electromagnetic waves.
Attenuation:	The decrease in magnitude experienced by an electromagnetic radiated wave or a conducted signal in traversing a transmission medium such as free space, a shielded enclosure, or a filter. Attenuation results from reflection, radiation and/or absorption and is expressed in dB.
Capacitance:	That property of a condenser which determines how much charge can be stored in it for a given potential difference across its terminals.
Capacitor:	A device used in a variety of electric circuits. For example, capacitors are used (1) to tune the frequency of radio receivers, (2) to eliminate sparking in automobile ignition systems, and (3) as short-term energy storing devices in electronic circuits.
Conducted emissions:	Desired or undesired electromagnetic energy propagated along a conductor.
Continuous wave:	An electromagnetic wave in which successive oscillations are identical under steady-state conditions
Current:	The rate at which a charge flows through a conductive surface.
Degradation:	In susceptibility testing, any undesirable change in the operational performance of a test specimen, This may not necessarily mean malfunction or failure.
Dielectric:	An insulating material, such as rubber, glass or waxed paper. When a dielectric is placed between power and ground plates, the capacitance increases.

EFS:	Electrical field strength is the magnitude of the electric field in an electromagnetic field.
EMC:	Electromagnetic Compatibility is the capability of electronic equipment or systems to operate, with a defined margin of safety, in the intended electromagnetic environment at designed levels of efficiency without causing degradation to its own or other systems because of interference.
EMI:	Electromagnetic Interference is an electromagnetic disturbance that causes or can cause undesired responses, malfunctioning, or degradation of performance of electrical or electronic equipment.
Emission:	Electromagnetic energy, produced by a device, that is radiated into space or conducted along wires and can be measured.
Farad (F):	The SI unit for capacitance.
FCC:	Federal Communication Commission establishes rules on emission control for electronic systems.
frequency:	The number of cycles per second of an alternating electric current.
Henry (H):	The SI system (System International) for measuring inductance.
Immunity threshold:	The maximum level of interference that can be tolerated by equipment under test without it showing an undesirable response, malfunction, or performance degradation beyond the stated tolerances.
Inductance:	The property of an electric circuit by which a varying current in it produces a varying magnetic field that induces voltages in the same circuit or a circuit in close proximity.
LCR meter:	Inductance, capacitance and resistance measuring device.
Noise:	For an interference-measuring instrument, the area divided by the height of the voltage response versus frequency curve, with the voltage measured from the antenna up to but not including the detector.
Oscilloscope:	Is an electronic instrument widely used in making electrical measurements.

Powers:

Power	Prefix	Abbreviation
10^{-18}	atto	a
10^{-15}	femto	f
10^{-12}	pico	p
10^{-9}	nano	n
10^{-6}	micro	μ
10^{-3}	milli	m
10^{-2}	centi	c
10	deca	d
10^{3}	kilo	k
10^{6}	mega	M
10^{9}	giga	G
10^{12}	tera	T
10^{15}	peta	P
10^{18}	exa	E

Random noise: An undesirable, high frequency disturbance in an electrical system that modifies or affects the performance of a desired signal.

Resonance frequency: The frequency reached in a series circuit when the current has its maximum value.

Spectrum analyzer: An electrical measurement device used to measure noise pulses in a wide frequency range.

A.3 Buried Capacitance Evaluation Form

This appendix contains the Buried Capacitance™ Inquiry. This is utilized to assist in determining how to utilize the BC-2000 buried capacitance material effectively.

Buried Capacitance™ Inquiry
BC-2000™ Laminate

Date:		**Name:**	
Company:		**Title:**	
Address:		**Phone:**	
City:		**Fax:**	
State / Zip:		**Email:**	

1. What is the part number under review? _____

   What is the product application? Networking etc._____

   _____

2. Current board size (overall dimensions in inches). _____

3. Board logic type. ☐ digital ☐ analog ☐ combination. Please explain.

   _____

4. Approximate area of the digital plane, if the planes are split or segmented._____Sq. inches.

5. Frequency (MHz) and rise time (Nanoseconds) appropriate for your application. _____

6. Percentage of components on subject board that are discrete bypass capacitors._____

7. Discrete bypass capacitor values currently being used. Please note that .1µF is the largest bypass capacitor type that BC can replace. List other values and qty's as needed.

Value	.1µF	.01µF	.001µF			
Qty.						

8. Does the design incorporate a section of memory?
   ☐ Yes ☐ No
   Please explain. _____

9. Voltages being used on the voltage planes. _____

10. Please indicate the current lay up, controlled impedance values, if any, that must be maintained and intended line and space.
    Show all layer names. i.e. S-Sig., P-Pwr., G-Gnd. etc.

Layer	Description	Impedance Ω	Line/Space
1			/
2			/
3			/
4			/
5			/
6			/
7			/
8			/
9			/
10			/
11			/
12			/
13			/
14			/
15			/
16			/

11. Current board thickness. _____
    _____
    How is thickness measured? i.e. over tips, over solder mask.____
    _____

12. EMI requirements that this product will be required to meet. _____
    _____
    _____
    Please List FCC Class A, Class B, VDE, European Standards, etc.

13. Any special environmental requirements? ☐ No ☐ Yes
    Please explain._____
    _____
    _____

14. An EMI compliance engineer that we may contact at your company.

    Name. _____ Phone. _____

15. Was Buried Capacitance recommended by an industry consultant or another company?
    By whom? _____
    Company? _____

16. List in priority sequence (1 is first priority) your primary reason for using Buried Capacitance.

	EMI noise reduction
	Quality/reliability improvement
	Signal integrity improvement
	Faster design routing
	Cost reductions
	Reduced assembly time - increased throughput
	Ability to add more functionality to board
	Size reduction
	Shorter development cycle
	Faster time to market

Please fax the completed questionnaire to your SANMINA Field Application Engineer or Rep

Special Notes Area